

Figure 1. PRIOR ART

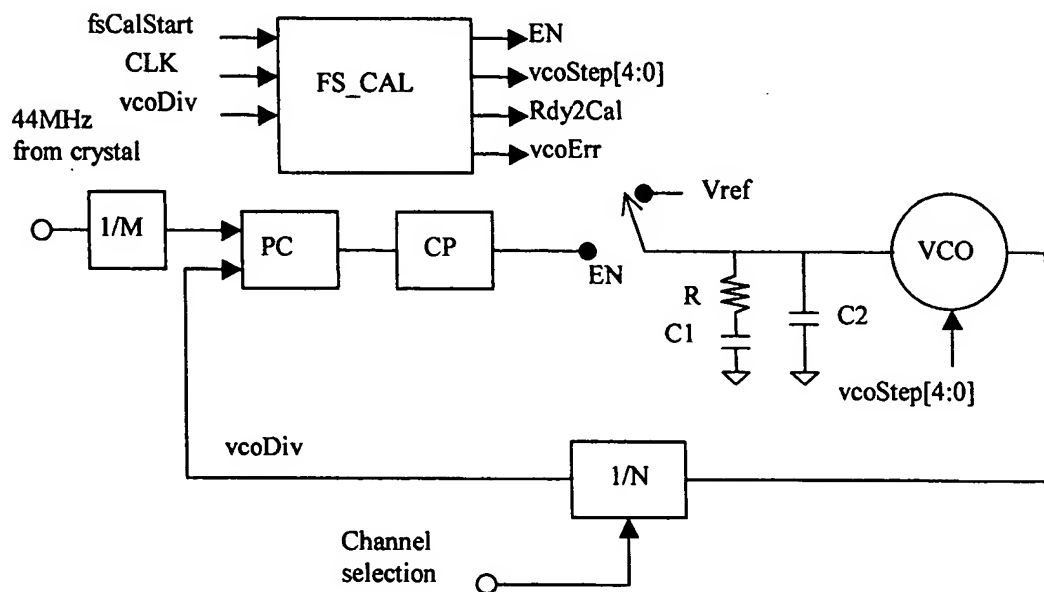


Figure 2.

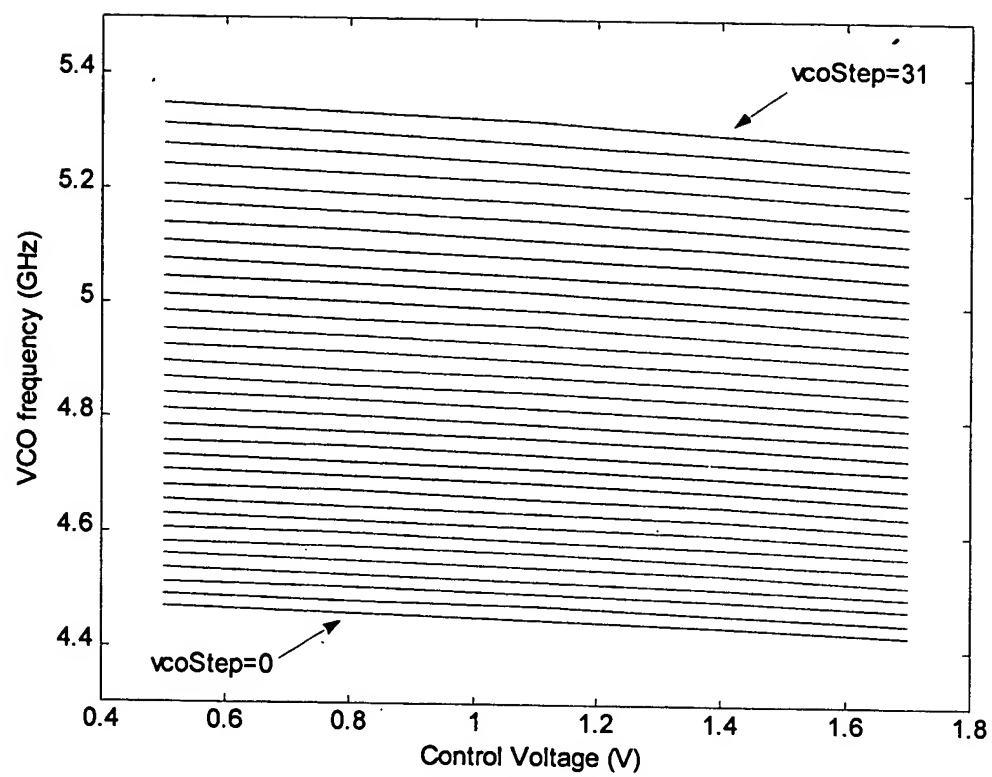


Figure 3

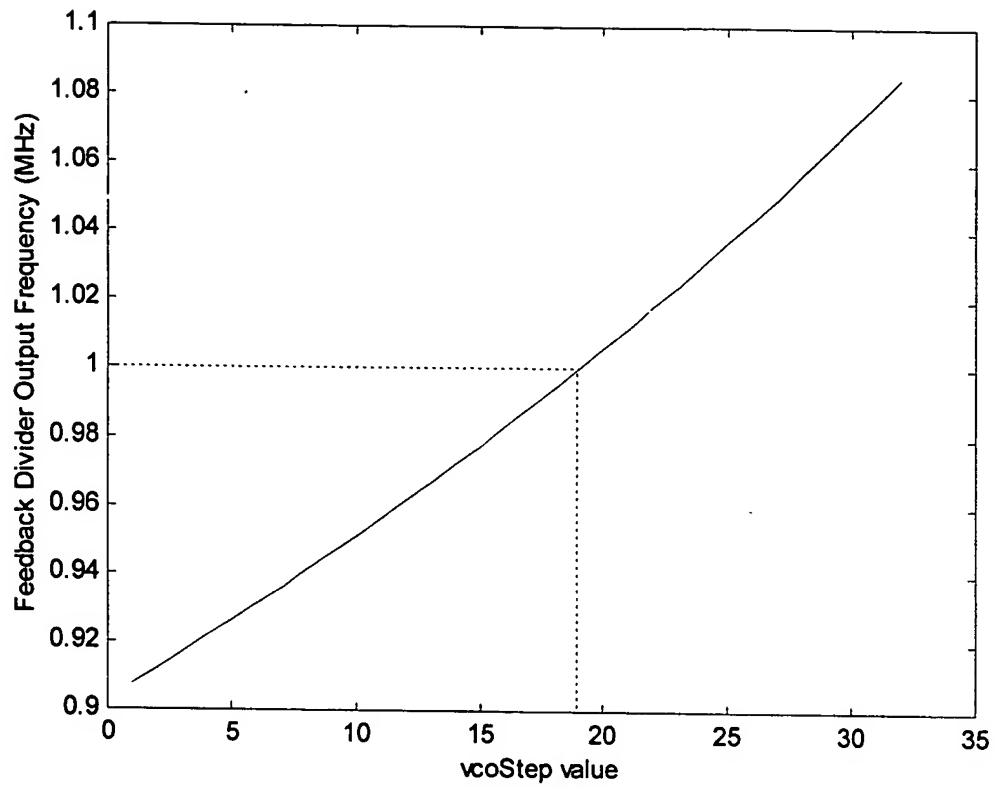


Figure 4.

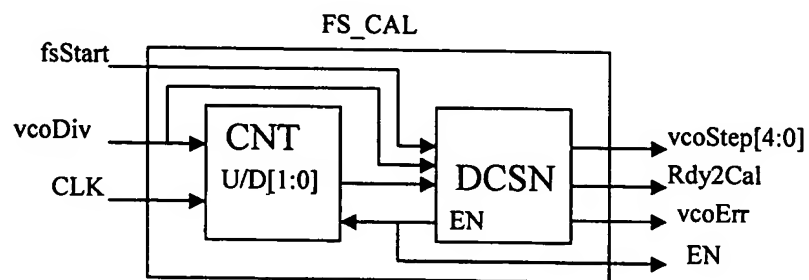


Figure 5.

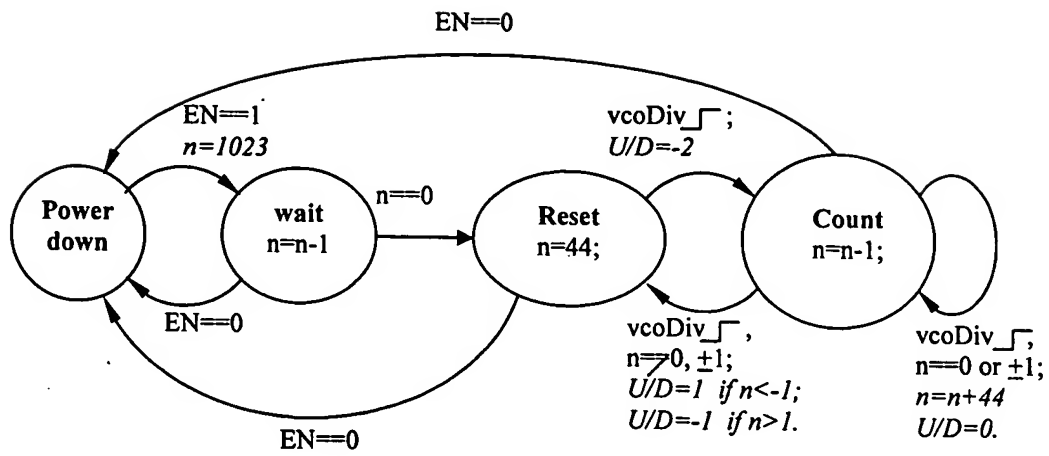


Figure 6.

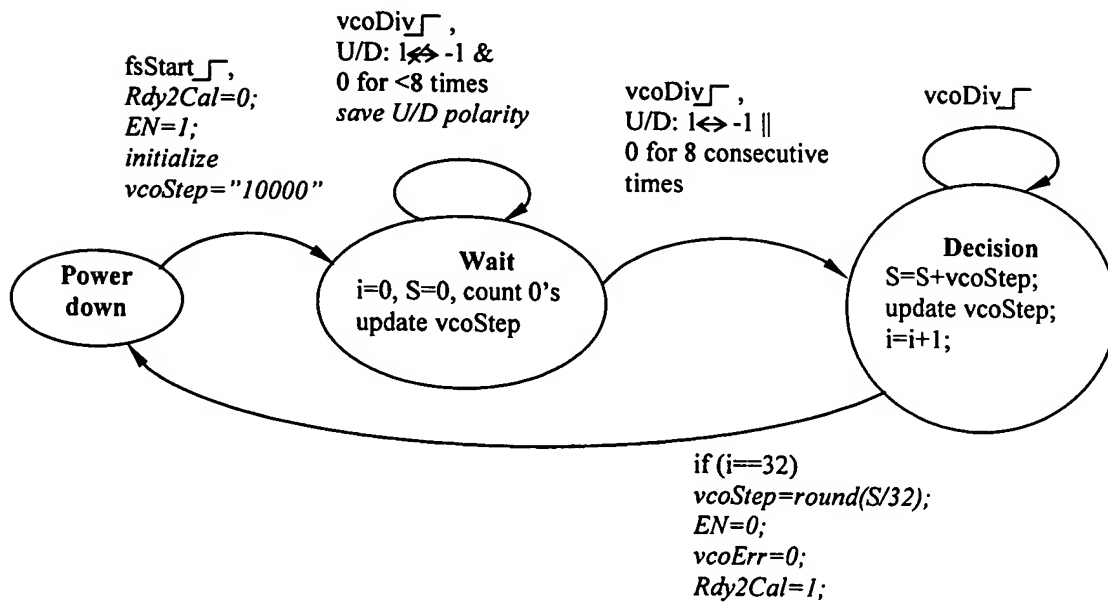


Figure 7.

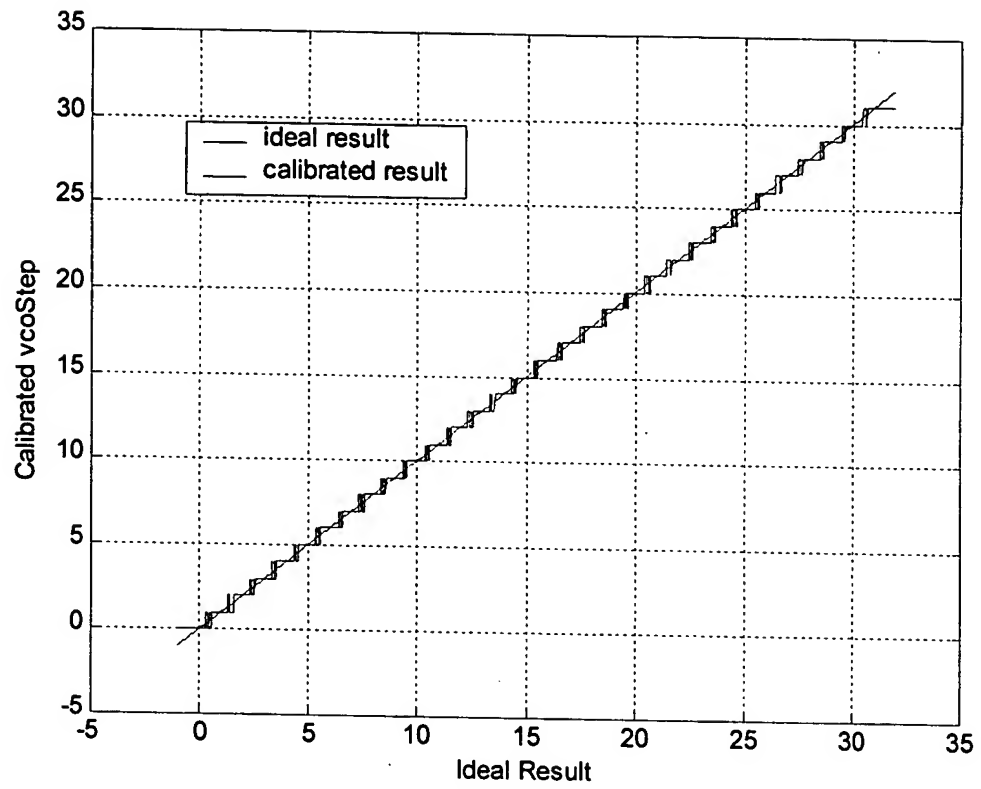


Figure 8.

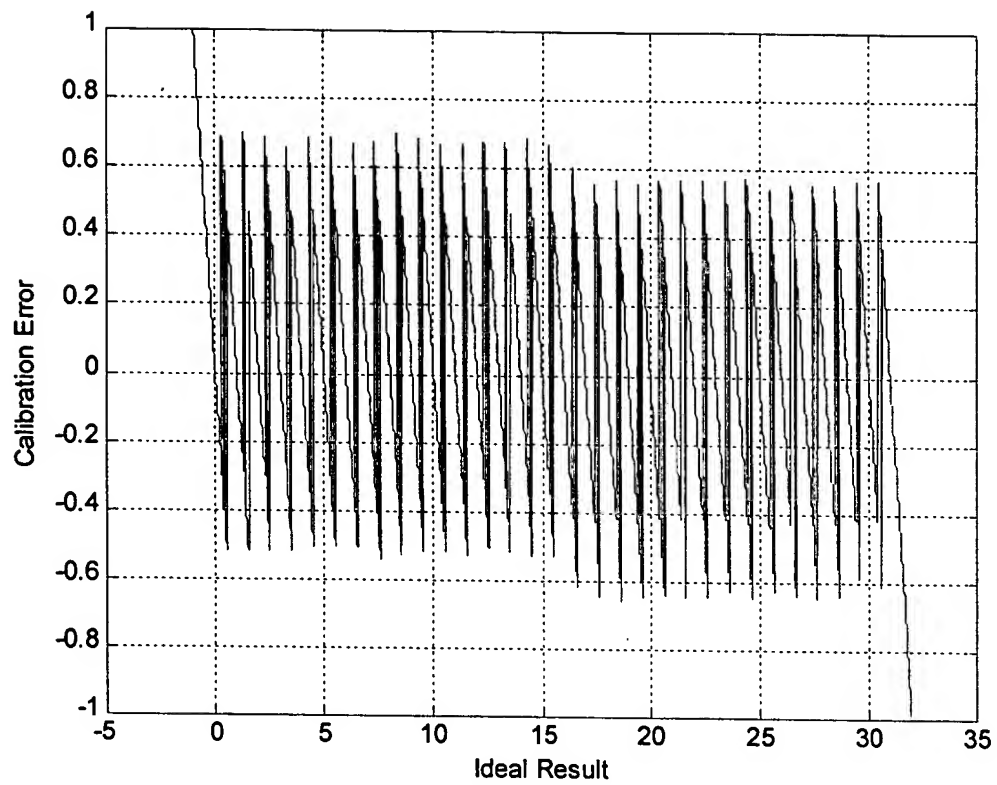


Figure 9.

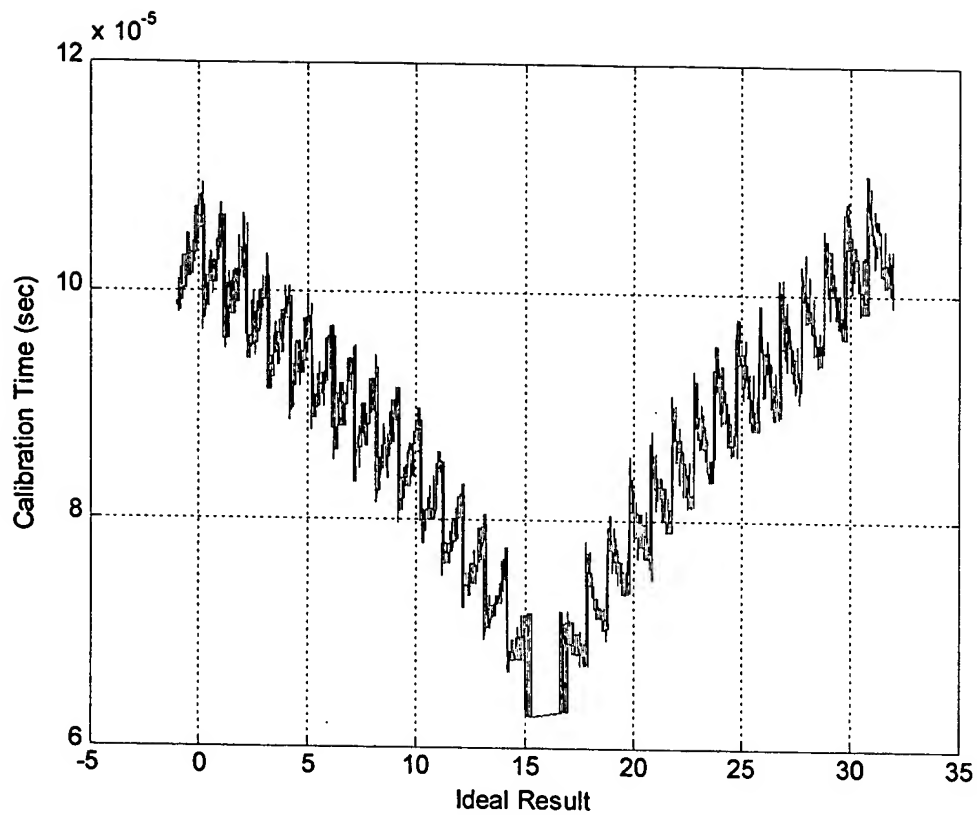


Figure 10.

Pin	I/O	Description
fsStart	I	Rising edge triggers the start of the calibration.
vcoDiv	I	VCO feedback divider output, frequency close to 1MHz, depending on vcoStep[4:0].
CLK	I	44MHz clock from crystal oscillator
vcoStep[4:0]	O	VCO frequency control, "00000": lowest frequency, "11111": highest frequency; default: "10000"
Rdy2Cal	O	'1': VCO calibrated; '0': VCO not calibrated; default: '1'
vcoErr	O	'1': VCO calibrated with error; '0': VCO calibrated without error; default: '0'
EN	O	'1': enables CNT, puts PLL into calibration; '0': disables CNT, puts PLL into normal operation; default: '0'
U/D[1:0]	N/A	+1: increment vcoStep; -1: decrement vcoStep; 0: remain unchanged; -2: waiting, remain unchanged

Table 1.